
Actions

MICROELECTRONICS Co., Ltd.

AM8962DR Datasheet

Document Number: AM8962DR Datasheet

Revision 1.0.2

Release date: 2026/09/15

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Revision History

Version	Date	Description	Author
1.0	2026/04/24	Initial Create	yinshanshan
1.0.1	2026/09/08	Review: 1. All power 2. Sequence Diagram 3. Features	Caozhirui LIZhang
1.0.2	2026/09/15	Technical review & document polishing	WT

General Conventions

Symbol	Description	Notes
Note		
H	In the notes column, an H indicates the pin is hidden behind the actual physical pin listed in the Alternate Functions column and is not included in the pin count. No H indicates the actual pin is listed in the Signal Name column and the Alternate Functions column lists the alternate signals present on the pin.	
Pad GP		
1	Pad group 1	
2	Pad group 2	
Dir/Pol (direction/polarity)		
I	Input	
O	Output	
B	Bidirectional	
Z	Three state output	
Pad Type		
A	Analog pad	
B	Bidirectional	
BS	Bidirectional with Schmitt trigger	
H	High-voltage(up to 3.0 V)tolerant digital input	
I	CMOS input	
IA	Analog input	
IS	Input with Schmitt trigger	
K	Contains an internal weak keeper device	
O	Output	
OA	Analog output	
OD	Open-drain	
PD	Contains an internal pull-down device	
PP[NP]	Can be programmed to non pull, pull down or pull up. The default value is no pull after reset.	
PP[PD]	Can be programmed to non pull, pull down or pull up. The default value is pull down after reset.	
PP[PU]	Can be programmed to non pull, pull down or pull up. The default value is pull up after reset.	
PU	Contains an internal pull-up device	
PWR	power	
Z	High-Z output	
Drive (mA)		

n	Variable drive strength pins.	
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ACTIONS-MICRO

Introduction

Overview

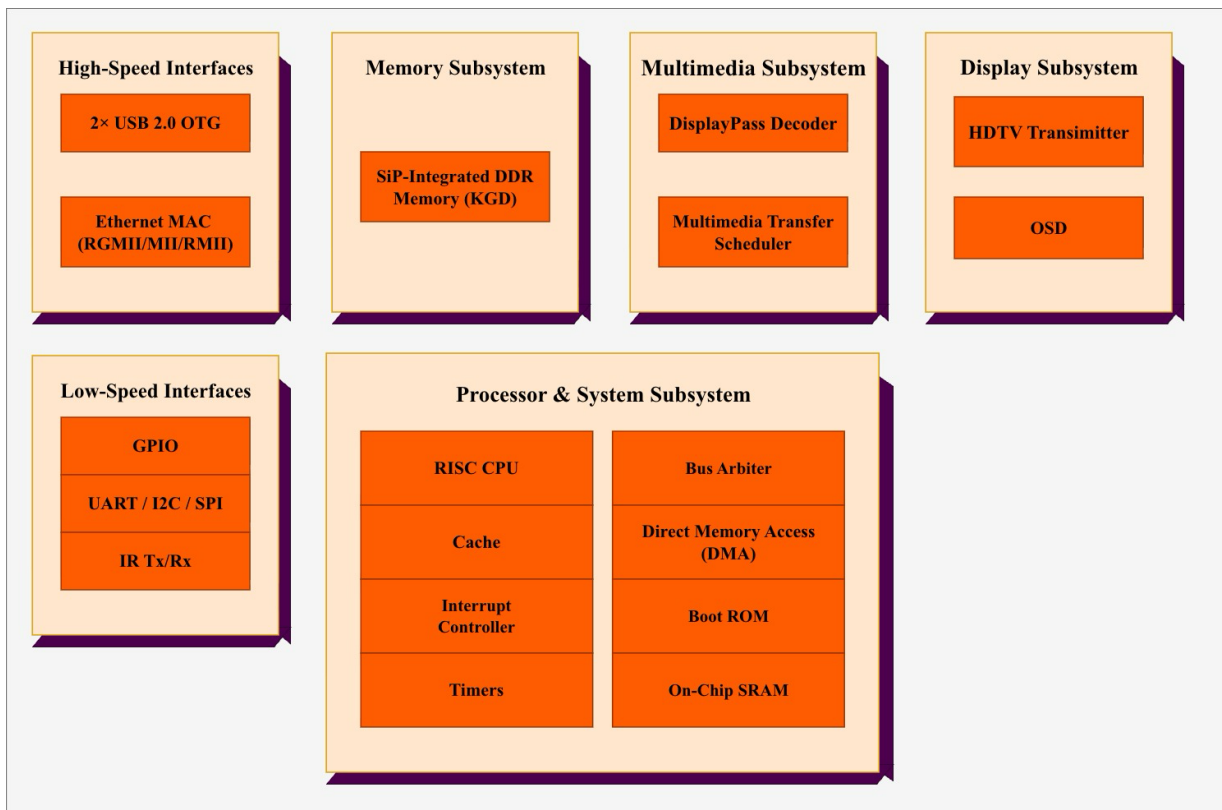
The AM8962DR from Actions Microelectronics is a highly integrated, mixed-signal multimedia processor SoC designed for high-performance wireless display reception and networked video playback. It embeds a 32-bit RISC CPU core with DSP instruction extensions operating at up to 1 GHz.

Designed for advanced wireless and networked video receiving applications, the SoC integrates a proprietary hardware **video decoder** engine compliant with DisplayPass Alliance specifications at up to 4K @ 60 fps, alongside a low-latency decompression engine capable of receiving 4K RGB888 video over 100-Mbps Fast Ethernet and Gigabit Ethernet interfaces.

The AM8962DR incorporates an on-chip HDTV 2.0 transmitter (TX) interface, directly driving high-resolution displays. Furthermore, the SoC features dual USB 2.0 controllers and a rich set of peripheral interfaces, including UART, I2C, and SPI.

Utilizing System-in-Package (SiP) technology, the processor embeds a high-performance DDR Known Good Die (KGD), eliminating external DRAM components and significantly optimizing PCB layout design.

Block Diagram



AM8962DR BLOCK DIAGRAM

Features

The AM8962DR provides high level of system integration to support a wide variety of applications. The features of the AM8962DR include:

✓ **32BIT RISC CORE**

- 32K byte instruction cache and data cache
- F/W can program from DC up to 1GHz transparently
- DSP instruction for multi-media acceleration
- Static design allows changing clock at run-time for power saving

✓ **VIDEO DECODER**

- 60 frames per second at 4096x2160 resolution DisplayPass Decoder

✓ **DISPLAY INTERFACE**

- HDTV support, industry standard compliance HDTV2.0

✓ **AUDIO**

- I2S interface
- Support 32 levels volume control

✓ **Ethernet MAC**

- Support MII/RMII/RGMII up to 1Gbps rate

✓ **Transfer Schedule Manager**

- Transfer compressed video/audio data through Ethernet
- The transferred video up to 4096x2160 60fs

✓ **DMA CONTROLLER**

- 8 physical channels and 4 bus channels
- Stride mode support
- Software configurable priority

✓ **Boot ROM**

- On chip boot ROM with boot loader
- The system could be loaded from SPI Nor flash

✓ **USB 2.0 OTG (2)**

- Complies with Universal Serial Bus Specification. Revision 2.0.
- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode.

- Supports full-speed or high-speed in peripheral mode.
- Supports USB Mass Storage Class Bulk-Only Transport Revision 1.0 as host or device.
- Configurable/programmable size of endpoints.
- Configurable/programmable single, double, triple or quad buffering.
- Programmable type of endpoints.
- Supports high-speed high-bandwidth ISO and Interrupt transfer.
- Supports suspend, resume and power managements function.

✓ **OTHER INTERFACE**

- UART/I2C/SPI
- 3 external interrupts
- 14 configurable GPIO shared with function pins